In the Claims:

1. (Currently Amended) A data processing system having:

at least one processor chip including a processor unit and an internal data cache, and

an interface [[which]] configured to ~~receives~~ receive data ~~to be written~~ from the processor chip, the interface further configured to ~~discarding~~ discard all the data to be written to an external memory received from the processor chip.

2. (Previously Presented) A data processing system according to claim 1 in which the interface is coupled to a memory, the interface passing data to the processor chip during initialization.

3. (Original) A data processing system according to claim 1 further including one or more further processing chips which have read/write access to external memory.

4. (Previously Presented) A method of operating a processing chip having a processor, an internal data cache and a cache controller for transmitting write instructions out of the integrated circuit, the method including discarding the write instructions and arranging for the program code operated by the processor to require only the data cache as memory.

5. (Previously Presented) A data processing system according to claim 1 wherein the at least one processor chip comprises exactly one processor chip.

6. (Previously Presented) A data processing system according to claim 1 wherein the at least one processor chip comprises two processor chips.

7. (Previously Presented) A data processing system according to claim 1 wherein the processor chip further includes an internal cache controller coupled between the internal data cache and the processor unit.

8. (Currently Amended) A data processing system comprising:

a processor chip including an internal processor coupled to an internal data cache;

an external memory; and

an interface coupled between the processor chip and the external memory, the interface configured to receive memory data from the external memory and transfer the memory data to the processor chip, the interface further configured to receive processor data from the processor chip and discard all the processor data to be written to the external memory.

9. (Previously Presented) The system of claim 8 and further comprising a control circuit coupled to the interface circuit, the control circuit providing a control signal to indicate whether data received by the interface should be discarded.

10. (Previously Presented) The system of claim 9 wherein the control circuit comprises a decoder.

11. (Previously Presented) The system of claim 8 and further comprising:

a second processor chip that includes an internal processor coupled to an internal cache; and

a second interface, wherein the second processor chip is coupled to the external memory through the second interface.

12. (Previously Presented) The system of claim 11 and further comprising a system bus coupled to the processor chip, the second processor chip, the interface, and the second interface.

13. (Previously Presented) The system of claim 12 and further comprising a third processor chip coupled to the system bus.

14. (Previously Presented) The system of claim 13 wherein the third processor chip comprises a master processing unit and wherein the processor chip and the second processor chip comprise slave processing units.

15. (Currently Amended) The system of claim 14 and further comprising a second external memory directly coupled to the system bus ~~without an interface coupled between the second external memory and the system bus~~.